A generic ML-enhanced controller that optimizes network application energy efficiency

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A simple network processing example

Packet



A simple network processing example





A simple network processing example





1. **Idle -** CPU low power sleep states



1. Idle - CPU low power sleep states



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Idle longer, slow CPU processing?

Web services with service-level objectives (SLO) i.e. 99% tail latency < 1 ms

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Latency



Our work: tuning of two hardware knobs 1) **interrupt coalescing (ITR)** and 2) **processor speeds (DVFS)** to reduce energy while maintaining SLO across diverse sets of hardware/software

1. Performance and Energy Study

Defining the measurement problem

- Intel Xeon E5-2690 @ 2.90 GHz
- Intel 82599ES 10-Gigabit SFI/SFP+ NIC







Data Collection Framework for Systems

- A. Instrumented on network interrupt path
- B. Per-core /procfs entry
- C. Agnostic across application/OS



Data Collection Results

- Explored up to 340 unique ITR, DVFS combinations
- Repeated up to 10 times for experimental stability
- Collected TBs of systems logs data
- Finding: Linux can save up to 50% energy while meeting SLO of memcached.



400

0

200

99% Tail Latency (usecs)

200

400 0

0.5

0

200

400

0



400 0

200

200

Packet Packet



Packet



Packet







Packet Packet







- 1. Reduces interrupt handling costs
- 2. Prolong idle period
- 3. Stabilizes per-interrupt work:
 - Enables DVFS to better control performanceenergy trade-offs



ITR

2. Mathematical Modeling and Fitting

Motivation

- Study reveals common and stable structure in response to changes to ITR, DVFS
- a formal way.

Implication is that one can model performance and energy profiles in

Modeling Result

e.g.

 $\Delta t = \frac{Z}{DVFS^{1+\alpha}} + (\phi * ITR)$. . .

- • •
- ...

Details: https://handong32.github.io/PhDThesis.pdf



Modeling Result

e.g.

. . .

. . .

 $\Delta t = \frac{Z}{DVFS^{1+\alpha}} + (\phi * ITR)$



policies can be made feasible.

Details: https://handong32.github.io/PhDThesis.pdf

3. Applying ML to ITR, DVFS tuning

Building Block: Sample Efficient Machine Learning e.g. Bayesian Optimization

Reduces number of samples to find some optimal configuration:



Bayesian Optimization Controller Motivating use case: in-memory KV stores

- Stable structure
- Repetitive request rates
- Times scale in hours/days



Yang et al. A large scale analysis of hundreds of in-memory cache clusters at Twitter. OSDI'20

Bayesian Optimization Controller



Applying Controller to Twitter cache-trace Dataset



Details: <u>https://research.redhat.com/blog/article/tuning-linux-kernel-policies-</u> for-energy-efficiency-with-machine-learning/

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Applying Controller to Twitter cache-trace Dataset



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Generality of ITR, DVFS

Node: N0 (Intel E5-2640, Mellanox 25GbE)



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Generality of ITR, DVFS

Node: N0 (Intel E5-2640, Mellanox 25GbE)



Node: N1 (Intel E5-2660, Solarflare 10GbE)

Future Work

- Currently limited to a single application on a single node:
 - Per-core ITR, DVFS, multiple SLOs
- Explore other ML techniques and reward functions
- Generality of **batching**:
 - Receive/Send buffer windows, disk readahead, NFS rsize, quantums, preemption granularity, writeback throttle, LRO/GRO, NAPI poll budget, swapiness, etc

Conclusion performance powersave 0 ---ondemand



Performance

-

Backups



Control packet batching behavior via *ethtool*:



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1. Set ITR value



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Control packet batching behavior via *ethtool*:

- 1. Set ITR value
- 2. Incoming packets are buffered on receive queue until ITR value has been reached
- 3. Network device asserts interrupt for packet processing



Processor speed: Dynamic Voltage Frequency Scaling (DVFS)

- $P = C * V^2 * f$
 - $^{\circ} P = dynamic power$
 - $^{\circ}$ C = switching capacitance
 - V = operational voltage
 - $^{o} f$ = operational frequency

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- 1. Set dynamically by Linux policy governors
- 2. Our work explores **static** frequencies on a per-workload basis

